UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,754	09/03/2003	Stephan G. Meier	5500-97500	3663

53806 7590 12/10/2008

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL (AMD)
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER	
DILLON, SAMUEL A	
ART UNIT	PAPER NUMBER
2185	
MAIL DATE	DELIVERY MODE
12/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/653,754	MEIER ET AL.	
	Examiner	Art Unit	
	SAMUEL DILLON	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 22, 2008 has been entered. Per the amendment, Claims 1, 2, 11, 13, 14, 21 and 23-29 have been amended.

I. RESPONSE TO AMENDMENT(S) / ARGUMENT(S)

2. In response to the amendment, the 35 U.S.C. 112 second paragraph rejection of Claim 29 as stated in the previous action are withdrawn.

3. Applicant's arguments with respect to the 35 U.S.C. 102(b) and 103(a) rejections of Claims 1-29 have been fully considered but they are **not persuasive**. The rejections have been upheld, and the Applicant directed below for traversal.

4. **The Applicant contends *(pg 10)* that Tran disclose predicting a first way to be hit in the cache for the first address responsive to the first value matching one of a plurality of values, wherein the one of the plurality of values is output from the first way of the memory.** The Examiner respectfully disagrees. Tran discloses predicting a first way to be hit in the cache for the first address (use portion of index to access way prediction array, step 104) responsive to the first value matching one of a plurality of values *(for a way value to be in the way prediction array, it must have been correct previously, so that specific way was compared in step 122 and either updated in step 124 or kept in step 126, figure 6; therefore, the outputting of a way from the way prediction array can be considered in response to it being added or kept in the way*

prediction array), wherein the one of the plurality of values is output from the first way of the memory *(step 104, figure 6)*. Accordingly, Tran does disclose the contested limitations.

5. **The Applicant appears to contend *(pg 10)* that Tran does not disclose the a tag memory as being part of the cache, and the memory storing the values as being separate from that tag memory.** The Examiner respectfully disagrees. Tran discloses a tag array as being part of the cache, and also a way prediction array that is separate from the tag array *(as described in figure 6)*. Accordingly, Tran does disclose the contested limitations.

6. Regarding all other Claims not specifically traversed above and whose rejections were upheld, the Applicant contends that the listed claims are allowable by virtue of their dependence on other allowable claims. As this dependence is the sole rationale put forth for the allowability of said dependent claims, the Applicant is directed to the Examiner's remarks above. Additionally, any other arguments the Applicant made that were not specifically addressed in this Office Action appeared to directly rely on an argument presented elsewhere in the Applicant's response that was traversed, rendered moot or found persuasive above.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102 - Tran

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claims 1-11, 13-21, 23, 27 and 28** are rejected under 35 U.S.C. 102(b) as being anticipated by Tran *(US Patent No. 6,016,533)*.

9. For **Claim 1**, Tran discloses a way predictor comprising:

a decoder configured to decode an indication of a first address that is to access a cache, the decoder configured to select a set responsive to the indication of the first address *(decoder is coupled to the memory locations and storage locations, and is configured to receive and decode addresses, col. 3, lines 24-29)*;

a memory coupled to the decoder, wherein the memory is configured to output a plurality of values from a set of storage locations in response to the decoder selecting the set, wherein each of the plurality of values corresponds to a different way of a plurality of ways of the memory *(the decoder may be configured to select a subset of way predictions from a selected set based upon a portion of a requested address, col. 3, lines 41-44)*, wherein the cache includes a same number of ways as the memory *(the way prediction can be any way, figure 3)* , and wherein the cache includes a tag memory storing a plurality of tags corresponding to cache lines stored in the cache and a data memory storing the cache lines *(tag array and data in memory, figure 6)*, wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line stored in the cache *(way prediction, figure 3)*; and

a circuit coupled to receive the plurality of values and a first value corresponding to the first address, wherein the circuit is configured to predict a first way of the plurality of ways to be a hit in the cache for the first address responsive to the first value matching one of the plurality of values *(the cache memory uses portions of the requested address in parallel to reduce way*

prediction, col. 3, lines 5-7; a first portion of a requested address is used to select a set of way predictions within the plurality of storage locations, col. 3, lines 22-24), and wherein the first way of the plurality of ways in the memory stores the one of the plurality of values *(way prediction array, step 104, figure 6)*.

10. For **Claim 2**, Tran discloses the circuit comprises a plurality of comparators, wherein each comparator of the plurality of comparators is configured to compare a respective one of the plurality of values to the first value, and wherein the circuit is configured to predict the first way of the cache for which the corresponding value of the plurality of values matches the first value as indicated by the plurality of comparators *(each array is coupled to receive a portion of a request address, and when data cache receives a requested address, a tag array uses an index portion of the requested address to access a particular set of tags, which are conveyed to a tag comparator, which receives a second portion of the requested address to compare with the selected set of tags; if one of the tags compares equal, there is a "hit" in the cache, and if none of the tags equal the second portion of the address, there is a "miss", col. 13, lines 10-20)*.

11. For **Claim 3**, Tran discloses the circuit, if none of the plurality of values matches the first value, is configured to assert an early miss signal *(the data cache is pipelined so that the next access is started before the validity of the previous way prediction is determined, col. 15, lines 31-40)*.

12. For **Claim 4**, Tran discloses each of the plurality of values comprises a portion of a tag identifying a corresponding cache line in the cache, the portion excluding at least one bit of the tag *(col. 3, lines 22-24; col. 13, lines 10-20; a cache line is read and output by the sense amp unit, if the requested address hits in the tag cache, the way prediction is verified by comparator which receives the way prediction after it is selected from way*

prediction array, col. 14, lines 34-39; offset bits from a request address are used to selected the requested bytes from the cache line, col. 14, lines 35-36).

13. For **Claim 5**, Tran discloses each of the plurality of values is derived from at least a portion of the indication of the address identifying a corresponding cache line *(col. 3, lines 22-24; col. 13, lines 10-20)*.

14. For **Claim 6**, Tran discloses each of the plurality of values comprises a portion of one or more address operands used to generate the address *(col. 3, lines 22-24; col. 13, lines 10-20)*.

15. For **Claim 7**, Tran discloses at least one bit of one of the plurality of values is a logical combination of two or more bits of the address *(a first portion of a requested address is used to select a set of way predictions stored within the plurality of storage locations.., a first subset of memory locations may be selected based upon a second portion of the requested address and the selected set of way predictions.., a second subset of memory locations may be selected based upon the third portion of the requested address.., in one embodiment, the second portion and third portion of said requested address may be the same portion of the requested address, col. 3, lines 22-44)*.

16. For **Claim 8**, Tran discloses at least one bit of one of the plurality of values is a logical combination of two or more bits of one or more address operands used to generate the address *(col. 3, lines 22-44)*.

17. For **Claim 9**, Tran discloses the indication of the first address comprises at least a portion of the first address *(col. 3, lines 22-24)*.

18. For **Claim 10**, Tran discloses the indication of the first address comprises two or more address operands used to generate the first address *(col. 3, lines 22-24)*.

19. For **Claim 11**, Tran discloses if the way prediction is incorrect, the cache is configured to replace a cache line in the way indicated by the way prediction with a missing cache line corresponding to the first address *(if there is no match found in the tags, a cache miss occurs, and the output data is canceled and the requested data is fetched from main memory, col. 15, lines 31-33)*.

20. **Claim 13** is rejected using rationale as per rejection of claim 1 above, where Tran discloses both a cache memory and corresponding elements *(col. 3, lines 19-67, col. 4, lines 1-4)* as well as a method for accessing a cache array and reading a plurality of way predictions from a way prediction array for use with the cache memory and corresponding elements *(col. 4, lines 5-24)*.

21. **Claim 14** is rejected using rationale as per rejection of claims 2 and 13 above.

22. **Claim 15** is rejected using rationale as per rejection of claims 3 and 14 above.

23. **Claim 16** is rejected using rationale as per rejection of claims 4 and 13 above.

24. **Claim 17** is rejected using rationale as per rejection of claims 5 and 13 above.

25. **Claim 18** is rejected using rationale as per rejection of claims 6 and 17 above.

26. **Claim 19** is rejected using rationale as per rejection of claims 7 and 17 above.

27. **Claim 20** is rejected using rationale as per rejection of claims 8 and 17 above.

28. **Claim 21** is rejected using rationale as per rejection of claims 11 and 13 above.

29. For **Claim 23**, Tran discloses an apparatus comprising:

a way predictor *(a cache memory employing way prediction, col. 3, lines 4-5)* comprising:

a decoder configured to decode an indication of a first address that is to access a cache, the decoder configured to select a set responsive to the indication of the first address *(col. 3, lines 24-29)*;

a memory coupled to the decoder, wherein the memory is configured to output a plurality of values from the set in response to the decoder selecting the set, wherein each of the plurality of values corresponds to a different way of a plurality of ways of the memory, wherein the cache includes a same number of ways as the memory *(the way prediction can be any way, figure 3)* , and wherein the cache includes a tag memory storing a plurality of tags corresponding to cache lines stored in the cache and a data memory storing the cache lines *(tag array and data in memory, figure 6)*, wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line in the cache *(col. 3, lines 41-44)*; and

a first circuit coupled to receive the plurality of values and a first value corresponding to the first address, wherein the first circuit is configured to predict a first way of the plurality of ways to be a hit in the cache for the first address responsive to the first value matching one of the plurality of values, and wherein the first way of the plurality of ways in the memory stores the one of the plurality of ways *(col, 3, lines 5-7; col. 3, lines 22-24)*; and

the data cache data memory coupled to the way predictor, wherein the data cache data memory is arranged into the plurality of ways, and wherein the data cache data memory is configured to output data from the first way, and wherein the predicted way is identified by the way prediction *(data cache is a high speed cache memory provided to temporarily store data being transferred between load/store unit and the main memory subsystem, and may employ a way prediction mechanism, col. 10, lines 55-63)*, and wherein the data cache data memory includes a second circuit configured to reduce power consumption attributable to one or more non- predicted ways of the plurality of ways *(die*

space and power consumption may be reduced through the use of one sense amp unit instead of multiple sense amp units, i.e., one sense amp unit per way or Column, col. 3, lines 8-16).

30. For **Claim 24**, Tran discloses the data cache tag memory configured to output a tag from the first way *(a tag array uses an index portion of the requested address to access a particular set of tags, which are conveyed to a tag comparator, which receives a second portion of the requested address to compare with the selected set of tags; if one of the tags compares equal, there is a "hit" in the cache, and if none of the tags equal the second portion of the address, there is a "miss", col. 13, lines 10-20)*. Tran does not explicitly disclose not outputting tags from the one or more non- predicted ways, however, this is inherently true in Tran's disclosure. It is only when there is a hit or a correct prediction in the cache that a tag is output and used, therefore a miss or a non-predicted way would, inherently not produce a tag to be used.

31. For **Claim 25**, Tran discloses the second circuit is configured to generate separate wordlines for each of the plurality of ways in the data cache data memory, and wherein the second circuit is configured to activate a first wordline to the first way and to not activate word lines to the non-predicted ways *(fig. 3, items 50, 52, 54, 56; the data cache comprises a data arrayof a plurality of memory locations configured into columns, and each column is coupled to a corresponding sense amp unit, each which are coupled to way selection multiplexer and sense amp enable unit, col. 12, lines 20-25)*.

32. For **Claim 26**, Tran discloses the second circuit includes column multiplexor circuitry coupled to the plurality of ways and configured to select the output of the first way as input to a sense amplifier circuit, wherein the column multiplexor circuitry is controlled by the predicted first way *(col. 12, lines 20-25)*.

33. For **Claim 27**, Tran discloses the second circuit includes column multiplexor circuitry coupled to the plurality of ways and configured to select the output of the first way as input to a sense amplifier circuit, wherein the column multiplexor circuitry is controlled by the predicted first way *(col. 12, lines 20-25)*.

34. For **Claim 28**, Tran discloses the second circuit comprises a plurality of sense amplifier circuits, wherein each of the plurality of sense amplifier circuits is coupled to a respective one of the plurality of ways, and wherein each of the plurality of sense amplifier circuits includes an enable input that is controlled by the predicted first way*(data from one memory location is then selected for output by way selection multiplexer, which selects a particular column based upon a way prediction read from way prediction array, and the memory location at the intersection of the selected row and column is then read and output, col. 12, lines 39-44)*.

35. For **Claim 29**, Tran discloses the apparatus further comprising a second level cache *(the Examiner takes official notice that a second level cache is notoriously well known in the art, and that it would have been obvious to include a second level cache for the benefit of additional caching)*, and wherein the circuit is configured to detect a miss responsive to the plurality of values and the first value prior to the miss being detected in the cache that corresponds to the data cache data memory *(a miss that happened prior to the current access, possibly unrelated, column 1 lines 40-57)*, and wherein the circuit is configured to signal the miss to the second level cache, and wherein the second level cache is configured to begin an access corresponding to the first address responsive to signal from the circuit *(reading a value form a cache, column 1 lines 40-57)*.

Claim Rejections - 35 USC ' 103 – Tran and Wickeraad

36. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

37. **Claims 12 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran *(US Patent No. 6,016,533)* in view of Wickeraad et al *(US Patent No. 6,4901654)*.

38. For **Claim 12**, Tran fails to disclose if no way prediction is generated and a cache miss results for the first address, the cache is configured to use a replacement algorithm to select the cache line to be replaced with the missing cache line.

Wickeraad discloses a cache memory replacement algorithm that replaces cache lines based on the likelihood that cache lines will not be needed soon *(col. 4, lines 50-52)*.

Tran and Wickeraad are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Wickeraad suggests that it would have been desirable to incorporate a cache line replacement algorithm into the system of Tran because this allows data which is likely needed soon is assigned a higher replacement class, while data that is more speculative and less likely to be needed soon is assigned a lower replacement class *(col. 5, lines 2-6)*. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Tran as suggested by Wickeraad to incorporate the feature as claimed.

39. **Claim 22** is rejected using rationale as per rejection of Claims 12 and 21 above.

III. CLOSING COMMENTS

a. STATUS OF CLAIMS IN THE APPLICATION

40. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(1). CLAIMS REJECTED IN THE APPLICATION

41. Per the instant office action, Claims 1-29 have received an action on the merits and are subject of a non-final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 9:30-6:00.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

IMPORTANT NOTE

44. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sam Dillon
Examiner
Art Unit 2185

/SAD/

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185